

June 2002 Revised October 2002

FST32X245 16-Bit Bus Switch

General Description

The Fairchild Switch FST32X245 provides 16-bits of high speed CMOS TTL-compatible bus switching in a standard flow-through mode. The low On Resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device is organized as a 16-bit switch. When \overline{OE} is LOW, the switch is ON and Port A is connected to Port B. When \overline{OE} is HIGH, the switch is OPEN and a high-impedance state exists between the two ports.

Features

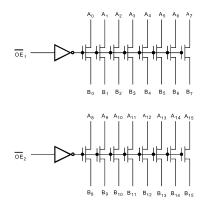
- \blacksquare 4 Ω switch connection between two ports
- Minimal propagation delay through the switch
- Low I_{CC}
- Zero bounce in flow-through mode
- Control inputs compatible with TTL level
- 16-bit version of FST3245

Ordering Code:

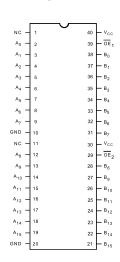
| Order Number | Package Number | Package Description | | | | |
|--------------|-------------------|--|--|--|--|--|
| FST32X245QSP | MQA40A | 40-Lead Quarter Size Very Small Outline Package (QVSOP), JEDEC MO-154, 0.150" Wide | | | | |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram



Connection Diagram



Pin Descriptions

| Pin Name | Description | | | | |
|----------------|-------------------|--|--|--|--|
| <u>OE</u> n | Bus Switch Enable | | | | |
| A _n | Bus A | | | | |
| B _n | Bus B | | | | |
| NC | No Connect | | | | |

Function Table

| Input OE _n | Function | | | |
|-----------------------|------------|--|--|--|
| L | Connect | | | |
| Н | Disconnect | | | |

Absolute Maximum Ratings(Note 1)

| Supply Voltage (V _{CC}) | -0.5V to $+7.0V$ |
|--|------------------|
| DC Switch Voltage (V _S) | -0.5V to $+7.0V$ |
| DC Input Voltage (V _{IN}) (Note 2) | -0.5V to $+7.0V$ |
| DC Input Diode Current (I_{IK}) V_{IN} < 0V | -50mA |
| DC Output (I _{OUT}) Sink Current | 128mA |
| DC V _{CC} /GND Current (I _{CC} /I _{GND}) | +/- 100mA |
| Storage Temperature Range (T _{STG}) | -65°C to +150 °C |

Recommended Operating Conditions (Note 3)

 $\begin{array}{ll} \mbox{Power Supply Operating (V_{CC})} & 4.0 \mbox{V to } 5.5 \mbox{V} \\ \mbox{Input Voltage (V_{IN})} & 0 \mbox{V to } 5.5 \mbox{V} \\ \mbox{Output Voltage (V_{OUT})} & 0 \mbox{V to } 5.5 \mbox{V} \\ \end{array}$

Input Rise and Fall Time (t_r, t_f)

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held HIGH or LOW. They may not float

DC Electrical Characteristics

| | | v _{cc} (V) | $T_A = -40 ^{\circ}\text{C} \text{ to } +85 ^{\circ}\text{C}$ | | | | |
|------------------|---------------------------------------|------------------------|---|-----------------|------|-------|---|
| Symbol | Parameter | | Min | Typ (Note 4) | Max | Units | Conditions |
| V _{IK} | Clamp Diode Voltage | 4.5 | | | -1.2 | V | I _{IN} = -18 mA |
| V _{IH} | HIGH Level Input Voltage | 4.0-5.5 | 2.0 | | | V | |
| V _{IL} | LOW Level Input Voltage | 4.0-5.5 | | | 0.8 | V | |
| I _I | Input Leakage Current | 5.5 | | | ±1.0 | μΑ | 0 ≤ V _{IN} ≤ 5.5V |
| | | 0 | | | 10 | μΑ | V _{IN} = 5.5V |
| I _{OZ} | OFF-STATE Leakage Current | 5.5 | | | ±1.0 | μΑ | 0 ≤ A, B ≤ V _{CC} |
| R _{ON} | Switch On Resistance | 4.5 | | 4 | 7 | Ω | V _{IN} = 0V, I _{IN} = 64 mA |
| | (Note 5) | 4.5 | | 4 | 7 | Ω | $V_{IN} = 0V$, $I_{IN} = 30 \text{ mA}$ |
| | | 4.5 | | 8 | 15 | Ω | $V_{IN} = 2.4V, I_{IN} = 15 \text{ mA}$ |
| | | 4.0 | | 11 | 20 | Ω | $V_{IN} = 2.4V, I_{IN} = 15 \text{ mA}$ |
| Icc | Quiescent Supply Current (Note 6) | 5.5 | | | 3 | μΑ | $V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$ |
| ΔI _{CC} | Increase in I _{CC} per Input | 5.5 | | | 2.5 | mA | One Input at 3.4V |
| | (Note 7) | | | | | | Other Inputs at V _{CC} or GND |

Note 4: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 5: Measured by the voltage drop between A and B pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B) pins.

Note 6: Per $V_{\rm CC}$ pin.

Note 7: Per TTL driven input, control pins only.

AC Electrical Characteristics

| | | $T_A = -40$ °C to +85 °C, $C_L = 50$ pF, RU = RD = 500Ω | | | | | | Figure |
|-------------------------------------|---------------------------------------|---|------|------------------------|------|-------|--|-----------------|
| Symbol | Parameter | V _{CC} = 4.5 - 5.5V | | V _{CC} = 4.0V | | Units | Conditions | Number |
| | | Min | Max | Min | Max | | | |
| t _{PHL} , t _{PLH} | Propagation Delay Bus to Bus (Note 8) | | 0.25 | | 0.25 | ns | V _I = OPEN | Figures 1, 2 |
| t _{PZH} , t _{PZL} | Output Enable Time | 1.5 | 5.9 | | 6.4 | ns | $V_I = 7V$ for t_{PZL} $V_I = OPEN$ for t_{PZH} | Figures 1, 2 |
| t _{PHZ} , t _{PLZ} | Output Disable Time | 1.5 | 6.0 | | 5.7 | | $V_I = 7V$ for t_{PLZ} $V_I = OPEN$ for t_{PHZ} | Figures 1, 2 |

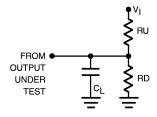
Note 8: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

Capacitance (Note 9)

| Symbol | Parameter | Тур | Max | Units | Conditions |
|------------------|-------------------------------|-----|-----|-------|-----------------------------------|
| C _{IN} | Control Pin Input Capacitance | 3 | | pF | $V_{CC} = 5.0V$ |
| C _{I/O} | Input/Output Capacitance | 5 | | pF | V_{CC} , $\overline{OE} = 5.0V$ |

Note 9: T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω Note: C_L includes load and stray capacitance Note: Input PRR = 1.0 MHz t_W = 500 ns

FIGURE 1. AC Test Circuit

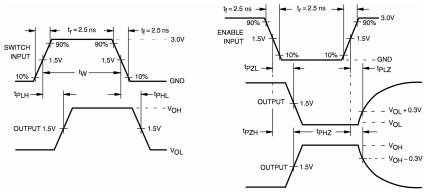
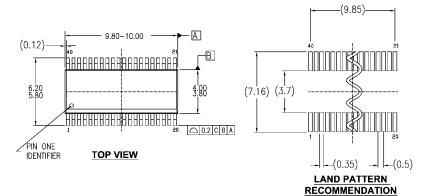
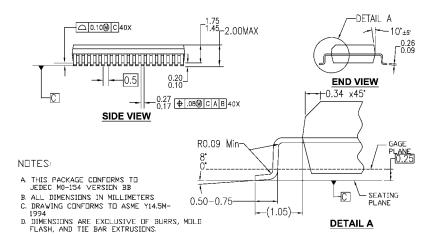


FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted





MQA40AREVA

40-Lead Quarter Size Very Small Outline Package (QVSOP), JEDEC MO-154, 0.150" Wide Package Number MQA40A

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